CLAIMS

1. A control apparatus for operating with program data, the apparatus comprising:

a first memory means that can read program data;

a second memory means that can write and read program data;

a writing means for writing data in the second memory means;

a selection means for selectively outputting an output from one of the first and second memory means; and

a control means for outputting a first address to one of the first and second memory means and operating with the output from the selection means as program data;

the selection means selecting the output from one of the first and second memory means in accordance with the first address;

the writing means enabling data to be written in the second memory means while operation of the control means is performed with the program data from the first memory means.

2. The control apparatus according to claim 1, wherein the control means includes a read address generation means for generating the first address for reading one of the first and second memory means, the read address generation means generating the first address so as to select the

output from one of the first and second memory means in accordance with the program data.

3. A control apparatus for operating with program data, the apparatus comprising:

a first memory means that can read program data;

a second memory means that can write and read program data;

a writing means for writing data in the second memory means;

a selection means for selectively outputting an output from one of the first and second memory means;

a control means for outputting a first address to one of the first and second memory means and operating with the output from the selection means as program data; and

a parameter memory means that can store a parameter therein;

the selection means selecting the output from one of the first and second memory means in accordance with the parameter;

the writing means enabling data to be written in the second memory means while operation of the control means is performed with the program data from the first memory means.

4. The control apparatus according to claim 3, and further comprising a read address generation means for generating the first address for reading one of the first and second memory means, the read address generation means generating the first address so as to select the output from one of the first and second memory means in accordance with the parameter stored in the parameter memory means.

5. The control apparatus according to claim 2, wherein the writing means includes a write address generation means for generating an address to be written in the second memory means, the writing means switching the output from the read address generation means and the output from the write address generation means in accordance with the output from the read address generation means and outputting the selected output to the second memory means.

6. The control apparatus according to claim 4, wherein the writing means includes a write address generation means for generating an address to be written in the second memory means, the writing means switching the output from the read address generation means and the output from the write address generation means in accordance with the output from the read address generation means and outputting the selected output to the second memory means.

7. The control apparatus according to claim 1, wherein a program is configured to arbitrarily switch the output from the first memory means and the output from the second memory means as program data.

8. The control apparatus according to claim 3, wherein a program is configured to arbitrarily switch the output from the first memory means and the output from the second memory means as program data.

9. The control apparatus according to claim 1, wherein one of the first and second memory means is a one-chip semiconductor element.

10. The control apparatus according to claim 3, wherein one of the first and second memory means is a one-chip semiconductor element.

11. The control apparatus according to claim 1, wherein the second memory means is a SRAM.

12. The control apparatus according to claim 3, wherein the second memory means is a SRAM.

13. A control apparatus for operating with program data, the apparatus including a one-chip semiconductor element comprising:

a first memory means for read only in which program data is written;

a second memory means that can write and read program data;

a writing means for writing data in the second memory means;

a selection means for selectively outputting an output from one of the first and second memory means; and

a control circuit for control operation in accordance with the output from the selection means;

the control apparatus enabling data to be written in the second memory means while the control circuit is performing control operation with the program data from the first memory means.

14. An optical disk apparatus for use with the control appartus according to claim 1, the optical disk apparatus comprising:

a system controller for outputting a control command to the control apparatus;

a spindle motor for rotation an optical disc at a predetermined speed;

an object lens for condensing a laser beam on the recording side of the optical disc;

an optical pickup for outputting a signal according to the amount of the reflected light from the optical disc, the optical pickup including an actuator for moving at least one of a laser light source and the object lens; and

a servo error signal generation circuit for generating a servo error signal by using the output signal from the optical pickup, and for supplying the servo error signal to the control apparatus;

the optical disk apparatus downloading program data from the system controller to the control apparatus and servo-controlling the servo error signal.

15. An optical disk apparatus for use with the control apparatus according to claim 3, the optical disk apparatus comprising:

a system controller for outputting a control command to the control apparatus;

a spindle motor for rotating an optical disc at a predetermined speed;

an object lens for condensing a laser beam on the recording side of the optical disc;

an optical pickup for outputting a signal according to the amount of the reflected light from the optical disc,

the optical pickup including an actuator for moving at least one of a laser light source and the object lens; and

a servo error signal generation circuit for generating a servo error signal by using the output signal from the optical pickup, and for supplying the servo error signal to the control apparatus;

the optical disk apparatus downloading program data from the system controller to the control apparatus and servo-controlling the servo error signal.

16. An optical disk apparatus for use with the control apparatus according to claim 13, the optical disk apparatus comprising:

a system controller for outputting a control command to the control apparatus;

a spindle motor for rotating an optical disc at a predetermined speed;

an object lens for condensing a laser beam on the recording side of the optical disc;

an optical pickup for outputting a signal according to the amount of the reflected light from the optical disc, the optical pickup including an actuator for moving at least one of a laser light source and the object lens; and

a servo error signal generation circuit for generating a servo error signal by using the output signal

from the optical pickup, and for supplying the servo error signal to the control apparatus;

the optical disk apparatus downloading program data from the ystem controller to the control apparatus and servo-controlling the servo error signal.

17. The control apparatus according to claim 2, wherein the writing means includes a write address generation means for generating a second address to be written to in the second memory means, the writing means selecting from between the first address and the second address in accordance with the first address and providing the selected address to the second memory means.

18. The control apparatus according to claim 4, wherein the writing means includes a write address generation means for generating a second address to be written to in the second memory means, the writing means selecting from between the first address and the second address in accordance with the first address and providing the selected address to the second memory means.